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EXAMINER

PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/877,792

Applicant(s)

SANCHEZ ET AL.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION***Specification***

1. The disclosure is objected to because of the following informalities: the term " $K_{10} \bullet C_{int} \bullet T_x$ " does not appear in equation 3, contradicting the specification at page 8, lines 19-26. The phrase "metallization resistant" at page 13, lines 1-4 is presumed to be a typographical error of "metallization resistance" and interferes with understanding the specification.
2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 1, 3, 9, 11, 15, 21, 22, 24, 29, 34, 36, and 37 recite the phrase "power supply voltage" which does not appear in the specification. Claims 1, 36, and 37 recite the phrase "distributed capacitance" which does not appear in the specification. Claims 1, 36, and 37 recite the phrase "distributed resistance" which does not appear in the specification. Claims 1 and 2 recite the phrase "running experiments using the performance model" which does not appear in the specification. Claim 7 recites the phrase "transistor impedance" which does not appear in the specification.

Appropriate correction is required.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the machine readable

medium of claim 36 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 1 is objected to because of the following informalities: The phrase "wherein the plurality constants are unknown constants" at page 29, lines 11-12 appears to contain a typographical error. Examiner presumes "wherein the plurality of

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constants are unknown constants" for the remainder of this action. Appropriate correction is required.

6. Claim 36 is objected to because of the following informalities: The phrases "A machine readable medium have stored therein information comprising" at page 34, line 17 and "where the plurality constants are unknown constants" at page 34, line 19 appear to contain typographical errors. Examiner presumes "A machine readable medium having stored therein information comprising" and "where the plurality of constants are unknown constants" for the remainder of this action.

7. Claim 37 is objected to because of the following informalities: The phrase "wherein the plurality constants are unknown constants" at page 35, lines 10-11 appears to contain a typographical error. Examiner presumes "wherein the plurality of constants are unknown constants" for the remainder of this action.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. § 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1-37 are rejected under 35 U.S.C. § 101.

10. Claims 1 and 37 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claims 1 and 37 recite a "process" for making an integrated circuit that makes reference to a mathematical result produced by prior recited steps. The connection between the step of making an integrated circuit

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and the prior mathematical steps is so tenuous that the claim, when considered as a whole, does not constitute a proper method under the statute. See *In re Sarker*, 200 USPQ 132 (CCPA 1978).

11. Claim 36 is rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claim 36 recites a machine readable medium having a stored program and limitations regarding the contents of the stored program and is therefore directed toward descriptive matter not claimed in conjunction with a tangible embodiment. See MPEP 2105 (IV)(B)(1).

12. Claims not specifically mentioned are rejected by virtue of their dependency.

13. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the first paragraph of 35 U.S.C. § 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

15. Claims 1-37 are rejected under 35 U.S.C. § 112, first paragraph, as based on a disclosure which is not enabling.

16. Claims 1, 36, and 37 recite the limitation of an equation which comprises a plurality of variables, one of which is related to transistor performance. The

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specification states that "the process parameter represents transistor performance fluctuations due to manufacturing process variations" (page 10, lines 23-24) but is silent as to what measurement is actually represented by the variable. The disclosure is devoid of examples where a variable related to transistor performance is specifically defined. Equation 3 (page 12) appears to be for calculating delay, presumably in a unit of time, however takes a process parameter as a variable. The disclosure provides no explanation regarding the dimensional analysis of equation 3 such that manufacturing process variations, in whatever units by which they may be measured, are resolved to produce a unit of time. The limitation of a variable representing transistor performance is no more enabling than the suggestion that such a variable exists. A person of ordinary skill in the art could not make and use the claimed invention without undue experimentation because there is no indication what is represented by the process parameter. Appropriate correction is required.

17. Additionally, claims 3, 9, and 10 recite limitations related to transistor performance.

18. Claims 14, 21, 23, 24, 28, and 34 recite limitations related to "transistor process technology", interpreted as functionally equivalent to "transistor performance", and are rejected for reasons similar to those given for claims 1, 3, 9, 10, 36, and 37 above.

19. Claims 1 and 37 recite the step of making an integrated circuit. Manufacturing an integrated circuit is critical or essential to the practice of the invention, but not included in the claim(s) is any limitation on the methods employed to make the integrated circuit. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The disclosure states

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that "Once the design is complete, an integrated circuit may be manufactured (block 818)" (page 26, lines 10-11), but is silent as to how an integrated circuit is made. Integrated circuit manufacture is a technology art unto itself. Indeed, applicant admits that integrated circuit manufacture is an ever-changing industry (page 1, lines 9-16). For computer-related inventions that involve more than one field of technology, the disclosure must satisfy the enablement standard for each aspect of the invention. See *In re Naquin*, 398 F.2d 863, 866, 158 USPQ 317, (319 CCPA 1968). The disclosure is silent regarding the methods for making an integrated circuit. Appropriate correction is required.

20. Claims not specifically mentioned are rejected by virtue of their dependence.

21. Claims 1-37 are rejected under 35 U.S.C. § 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed. Evidence of concealment of the best mode is based upon equations 3-5 of the disclosure.

22. Equations 3-5 describe mathematical formulae consisting of a number of terms, all with unknown coefficients, for modeling the performance of an electronic circuit. Several of the terms have non-unity exponents while others terms are linear. The influence of the exponential terms on the result, due to the asymptotic behavior of exponential functions compared to linear functions, will overwhelm the influence of the linear terms. Additionally, there is no indication that any of the coefficients, once determined, will be non-zero and have literally no influence on the result.

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23. It is apparent to the examiner that applicant knew of a mode of practicing the invention that the inventor considered to be better than any other. Equations for delay, capacitance, and setup/hold times are known in the art. As applicant considers the equations 3-5 as an inventive feature, indicated by claims 4-35, applicant would have been motivated to distinguish the equation from those known in prior art. The result of including insignificant terms and corresponding unknown coefficients in equations 3-5 is a set of equations that are obfuscated in an attempt to appear novel while performing equivalently to those of prior art at any meaningful level of scrutiny.

24. The disclosure is written so as to convey that the equations given are an improvement over the prior art (page 2, lines 8-19) however no evidence of this assertion is given. A person of ordinary skill in the art could only practice the best mode of the invention by abandoning the equations of the disclosure and adopting the modeling equations known in the art and taught against by the instant application.

25. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

26. Claims 1-37 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

27. Regarding claims 1 and 37, it is unclear to the examiner how applicant's invention can derive a set of constants for the plurality of unknown constants in an equation that comprises a plurality of variables and unknown constants. If the values of

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the plurality of variables are mutable, it is unclear how the unknown constants can be solved. If some constants were known a priori, such as certain design rules or circuit geometry, then a basis would exist from which other constants could be resolved.

28. Regarding claims 5-9, the claim language is generally vague and as a result, it is impossible to ascertain the metes and bounds of the claimed invention. For example, it

is unclear whether the delay expression comprises "metallization resistance" or "metallization resistance delay" in claim 5. It is unclear whether the phrase "metallization resistance" is an adjective phrase related to "delay". Claims 6-9 have similar language.

29. Regarding claim 5, 7, and 8, it is unclear what is meant by "metallization capacitance delay". This phrase does not appear in the disclosure.

30. Regarding claim 6, it is unclear what is meant by "load capacitance delay". This phrase does not appear in the disclosure.

31. Regarding claim 10, it is unclear what is meant by "process delay". This phrase does not appear in the disclosure.

32. Claim 36 recites the limitation "replacing the unknown constants with the first set of constants" at page 34, lines 23-24. There is insufficient antecedent basis for the phrase "the first set of constants" in the claim. As a result, it is unclear how the performance model of the first circuit design can be formed. See claim interpretation below.

33. Further regarding claim 36, the limitations recite "a machine readable medium having stored therein information comprising means for replacing the unknown

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constants with the first set of constants to obtain a performance model of the first circuit design." It is unclear how information, being descriptive material, can constitute means for performing a function.

34. Claims not specifically mentioned are rejected by virtue of their dependence.

Claim Interpretation

35. In the interest of compact prosecution, examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

36. Regarding claims 1, 3, 9, 11, 15, 21, 22, 24, 29, 34, 36, and 37, the phrase "power supply voltage" is interpreted as "supply voltage (i.e. Vdd)" according to page 4, line 18 – page 5, line 3.

37. Regarding claims 1, 36, and 37, the phrase "distributed capacitance" is interpreted as "capacitance" according to page 6, lines 1-6.

38. Regarding claims 1, 36, and 37, the phrase "distributed resistance" is interpreted as "resistance" according to page 6, lines 1-6.

39. Regarding claims 1, 3, 9, 10, 36, and 37 the phrase "transistor performance" is interpreted as "an influence on transistor performance".

40. Regarding claims 14, 21, 23, 24, 28, and 34, the phrase "transistor process technology" is interpreted as "an influence on transistor performance".

41. Regarding claims 1 and 2, the phrase "running experiments" is interpreted as "performing timing analyses" according to page 25, lines 1-5.

42. Regarding claims 1 and 37, the phrase "applying the circuit simulator to the first circuit design to derive a first set of constants for the plurality of constants" is interpreted as "using a circuit simulator to produce data to derive a first set of constants for the plurality of constants" according to page 19, lines 3-5.

43. Regarding claims 1 and 37, the phrase "making an integrated circuit comprising the second circuit design" is interpreted in anticipation that applicant will amend the specification in order to enable this limitation as being well known in the art.

44. Regarding claims 1 and 37, the limitation "applying a circuit simulator to the first circuit design to derive a first set of constants for the plurality of constants" is interpreted as "using simulation data in the process of solving the plurality of constants" according to page 23, lines 6-22.

45. Regarding claim 5, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to resistance and a variable related to capacitance."

46. Regarding claim 6, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to resistance and a variable related to capacitance."

47. Regarding claim 7, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to transistor impedance and a variable related to metallization capacitance" in anticipation that applicant will amend the specification in order to provide proper antecedent basis for the limitation of "transistor impedance."

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48. Regarding claim 8, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to an influence on transistor performance and a variable related to metallization capacitance."

49. Regarding claim 9, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to an influence on transistor performance and a variable related to supply voltage."

50. Regarding claim 10, the limitations are interpreted as "wherein the delay expressions comprise: a variable related to supply voltage."

51. Regarding claim 36, examiner cannot interpret the limitations of the claim without relying on speculative assumptions. See *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962). The origin of "the first set of constants" is unclear, the method by which they are produced is unclear, and the tangible embodiment of the claimed invention is unknown.

52. In general, the state of the disclosure and claims in the instant application preclude a limitation-by-limitation assessment of the claimed invention compared to the prior art. Therefore prior art is applied under 35 U.S.C. §§ 102 and 103 in an attempt to expedite prosecution in anticipation of future amendments.

Claim Rejections - 35 USC § 102

53. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

54. Claims 1-3, 36, and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Salimi et al., US Patent No. 5,883,818.

55. Regarding claim 1, Salimi et al. teaches a method for making an integrated circuit (column 3, lines 32-33) comprising:

providing a circuit simulator having the capability to of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 3, lines 39-44; Fig. 3, reference 200);

providing a first circuit design (column 3, lines 32-38);

providing an equation which comprises a plurality of variables and coefficients (column 3, lines 44-46; column 4, lines 22-46), wherein the plurality of coefficients are unknown coefficients (column 4, lines 47-51),

and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 4, lines 22-46);

applying the circuit simulator to the first circuit design to derive a first set of coefficients for the plurality of coefficients (column 3, lines 46-49; column 4, lines 47-51; column 5, lines 33-38; Fig. 3, reference 210);

replacing the unknown coefficients with the first set of coefficients to obtain a performance model of the first circuit design (column 3, lines 46-47; column 5, lines 33-38; Fig. 3, references 210, 220); running experiments using the performance model of the first circuit design (column 3, lines 47-49; Fig. 3, references 220, 230); changing the first circuit design to obtain a second circuit design (column 3, 59-64; column 5, lines 33-38; Fig. 3, references 220, 230, 240, 270, 290); making an integrated circuit comprising the second circuit design (column 5, lines 45-49; column 3, lines 32-38; column 4, lines 18-19).

Examiner considers that evaluating the performance of at least a portion of one of the logic cells at different operating parameters to generate simulation data (column 1, lines 56-58) is equivalent to providing and applying a simulator.

56. Regarding claim 2, Salami et al. teaches:

applying the circuit simulator to the second circuit design to derive a second set of coefficients for the plurality of coefficients (column 3, line 59 – column 4, line 1; column 5, lines 32-38; Fig. 3, references 220, 230, 240, 270, 290); replacing the first set of coefficients with the second set of coefficients to obtain a performance model of the second circuit design (column 3, line 59 – column 4, line 1; column 5, lines 32-38; Fig. 3, references 220, 230, 240, 270, 290); and

running experiments using the performance model of the second circuit design (column 3, line 59 – column 4, line 20; column 5, lines 32-38, Fig. 3, references 220, 230, 240, 270, 290).

57. Regarding claim 3, Salami et al. teaches that the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature (column 4, lines 22-46).

58. Claim 36 is directed toward a computer readable medium and recites limitations generally corresponding to the method of claim 1. As Salimi et al. teaches a system for designing an integrated circuit embodied on a computer (Fig. 1; column 2, line 58 – column 3, line 6), claim 36 is rejected for reasons similar to those given for claim 1 above.

59. Claim 37 is directed toward a method for obtaining a performance model and recites limitations generally corresponding to the limitations of claims 1 and 2. As Salimi et al. teaches a method for obtaining a performance model (column 3, lines 46-47; column 5, lines 33-38; Fig. 3, references 210, 220), claim 37 is rejected for reasons similar to those given for claims 1 and 2 above.

Claim Rejections - 35 USC § 103

60. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

61. Claims 1-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. US Patent No. 6,090,152 and further in view of Southgate US Patent No. 6,161,211.

62. Regarding claim 1, Hayes et al. teaches a method for predicting the performance of an integrated circuit design comprising:

providing a circuit simulator (column 6, lines 56-57) having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 6, lines 57-63);

providing a first circuit design (column 6, lines 45-53);

providing an equation which comprises a plurality of variables and coefficients (column 5, line 66 – column 6, lines 9);

wherein the plurality of coefficients are unknown coefficients (column 6, line 64 – column 7, line 12);

one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 5, line 66 – column 6, line 9);

applying the circuit simulator to the first circuit design to derive a first set of coefficients for the plurality of coefficients (column 6, line 64 – column 7, line 12); and

replacing the unknown coefficients with the first set of coefficients to obtain a performance model of the first circuit design and running experiments

using the performance model of the first circuit design (column 7, lines 13-28).

Hayes et al. does not teach changing the design of the circuit or making the circuit.

Southgate teaches a method for designing a circuit represented by blocks (column 5, line 66 – column 6, line 4; column 6, lines 30-38) wherein a performance analysis is conducted, and if goals for the design have not been met, changing the first circuit design to obtain a second circuit design and making an integrated circuit comprising the second circuit design (column 6, line 55 – column 7, line 9; Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to incorporate the redesign and manufacture steps of Southgate's invention into the circuit simulation and performance modeling method of Hayes et al. in order to produce a method that makes effective and efficient use of the results provided by the invention of Hayes et al. The combination could readily be achieved by making adjustments to the circuit design based on the modeling results and making the resulting integrated circuit by methods known in the art.

63. Regarding claim 2, Hayes et al. does not teach applying a circuit simulator to the second circuit design to derive a second set of coefficients, replacing the first set of coefficients with a second set of coefficients, and running experiments using the performance model of the second circuit design. However, the combination formed in

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the rejection of claim 1 anticipates this method. Having made adjustments to the circuit design based on the modeling results, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to subject the second circuit design to the same process as the first circuit design, and if it meets the performance goals, make a circuit according to the second design.

64. Performing this process with the invention of Hayes et al. would comprise: applying the circuit simulator to the second circuit design to derive a second set of coefficients for the plurality of coefficients; replacing the first set of coefficients with the second set of coefficients to obtain a performance model of the second circuit design; and running experiments using the performance model of the second circuit design.

65. Regarding claim 3, Hayes et al. teaches that the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature (column 5, line 66 – column 6, line 9; column 6, line 64 – column 7, line 12; column 7, lines 13-16; column 7, lines 37-41).

66. Regarding claims 4-12, Hayes et al. teaches that the equation comprises a plurality of delay expressions (column 5, line 35, equation 4; column 5, line 52, equation 5; column 5, lines 60-63, equation 6; column 6, lines 5-7, equation 7).

67. Claims 13-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. in view of Southgate as applied to claim 1 above, and further in view of Aingaran et al. US Patent No. 6,507,935.

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68. Regarding claims 13-24, neither Hayes et al. nor Southgate explicitly teach a plurality of capacitance expressions.

69. Aingaran et al. teaches a plurality of capacitance expressions (column 5, line 25 – column 6, line 60; column 11, lines 1-19). It would have been obvious for a person of ordinary skill in the art at the time of applicant's invention to combine the modeling equations of Aingaran et al. with the combined invention of Hayes et al. and Southgate in order to better simulate the performance of the circuit being designed.

70. Claims 25-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. in view of Southgate as applied to claim 1 above, and further in view of Misheloff, US Patent No. 5,559,715.

71. Regarding claims 25-35, neither Hayes et al. nor Southgate explicitly teach a plurality of setup/hold time expressions.

72. Misheloff teaches setup/hold time expressions (column 16, line 58 – column 17, line 21). It would have been obvious for a person of ordinary skill in the art at the time of applicant's invention to combine the modeling equations of Misheloff with the combined invention of Hayes et al. and Southgate in order to better simulate the performance of the circuit being designed.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

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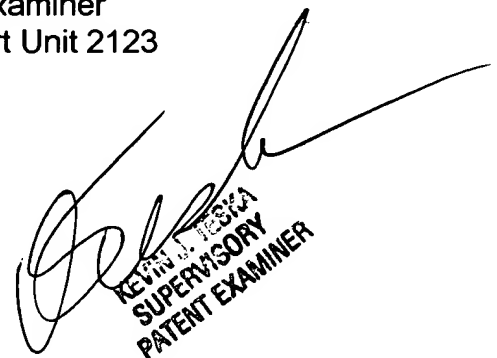
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (703) 305-0542 or (571) 272-3713 beginning in October 2004. The examiner can normally be reached on 8am-4pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704 or (571) 272-3716 beginning in October 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp



KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER